Results for "((interleave <and> arithmetic <and> 'and')<in>metadata)" e-mail
Your search matched **53** of **1166705** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History
» New Search

» Key

| | |
|---|---|
| IEEE JNL | IEEE Journal or Magazine |
| IEE JNL | IEE Journal or Magazine |
| IEEE CNF | IEEE Conference Proceeding |
| IEE CNF | IEE Conference Proceeding |
| IEEE STD | IEEE Standard |

Modify Search

((interleave <and> arithmetic <and> 'and')<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

Select Article Information View: 1

1. **114 MFLOPS logarithmic number system arithmetic unit for DSP applications**
Lewis, D.M.;
Solid-State Circuits Conference, 1995. Digest of Technical Papers. 42nd ISSCC, 1995 International
15-17 Feb. 1995 Page(s):86 - 87, 344
AbstractPlus | Full Text: PDF(720 KB) IEEE CNF

2. **Burst error recovery method for VF arithmetic codes**
Hongyuan Chen; Kitakami, M.; Fujiwara, E.;
Information Theory and Communications Workshop, 1999. Proceedings of the 1999 IE
20-25 June 1999 Page(s):124
AbstractPlus | Full Text: PDF(104 KB) IEEE CNF

3. **Interleaved memory function interpolators with application to an accurate LNS ar**
Lewis, D.M.;
Computers, IEEE Transactions on
Volume 43, Issue 8, Aug. 1994 Page(s):974 - 982
AbstractPlus | Full Text: PDF(776 KB) IEEE JNL

4. **Motion estimation using MSD-first processing**
Su, C.-L.; Jen, C.-W.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G- Circuits Systems]
Volume 150, Issue 2, April 2003 Page(s):124 - 133
AbstractPlus | Full Text: PDF(1537 KB) IEE JNL

5. **Interleaving entropy codes**
Howard, P.G.;
Compression and Complexity of Sequences 1997. Proceedings
11-13 June 1997 Page(s):45 - 55
AbstractPlus | Full Text: PDF(668 KB) IEEE CNF

6. **Area and time efficient modular multiplication of large integers**
Bunimov, V.; Schimmler, M.;
Application-Specific Systems, Architectures, and Processors, 2003. Proceedings. IEEE Conference on
24-26 June 2003 Page(s):400 - 409

AbstractPlus | Full Text: PDF(253 KB) IEEE CNF

7. **Multi-log processor - towards scalable event-driven multiprocessors**
Viswanath, V.;
Digital System Design, 2004. DSD 2004. Euromicro Symposium on
31 Aug.-3 Sept. 2004 Page(s):279 - 286
AbstractPlus | Full Text: PDF(436 KB) IEEE CNF

8. **Multithreading to improve cycle width and CPI in superpipelined superscalar pro**
Goossens, B.; Duc Thang Vu;
Parallel Architectures, Algorithms, and Networks, 1996. Proceedings. Second Internati
on
12-14 June 1996 Page(s):36 - 42
AbstractPlus | Full Text: PDF(684 KB) IEEE CNF

9. **Proceedings. Compression and Complexity of SEQUENCES 1997 (Cat. No.97TB1**
Compression and Complexity of Sequences 1997. Proceedings
11-13 June 1997
AbstractPlus | Full Text: PDF(144 KB) IEEE CNF

10. **Parametric spectral estimation on a single FPGA**
Bellis, S.; Marnane, W.; Fish, P.;
Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 1999 IEE
Conference on
Volume 4, 15-19 March 1999 Page(s):1973 - 1976 vol.4
AbstractPlus | Full Text: PDF(376 KB) IEEE CNF

11. **A simplified and efficient implementation of FPGA-based turbo decoder**
Sharma, S.; Attri, S.; Chauhan, F.C.;
Performance, Computing, and Communications Conference, 2003. Conference Proce
IEEE International
9-11 April 2003 Page(s):207 - 213
AbstractPlus | Full Text: PDF(691 KB) IEEE CNF

12. **114 MFLOPS logarithmic number system arithmetic unit for DSP applications**
Lewis, D.M.;
Solid-State Circuits, IEEE Journal of
Volume 30, Issue 12, Dec. 1995 Page(s):1547 - 1553
AbstractPlus | Full Text: PDF(816 KB) IEEE JNL

13. **Architecture of a high-rate VLSI Viterbi decoder**
Casseau, E.; Luthi, E.;
Electronics, Circuits, and Systems, 1996. ICECS '96., Proceedings of the Third IEEE Ir
Conference on
Volume 1, 13-16 Oct. 1996 Page(s):21 - 24 vol.1
AbstractPlus | Full Text: PDF(432 KB) IEEE CNF

14. **A 100-MHz 2-D discrete cosine transform core processor**
Uramoto, S.; Inoue, Y.; Takabatake, A.; Takeda, J.; Yamashita, H.; Terane, H.; Yoshim
Solid-State Circuits, IEEE Journal of
Volume 27, Issue 4, April 1992 Page(s):492 - 499
AbstractPlus | Full Text: PDF(752 KB) IEEE JNL

15. **Compaction of ordered dithered images with arithmetic coding**
Yinyi Lin; Wang, Y.J.; Fan, T.H.;
Image Processing, IEEE Transactions on
Volume 10, Issue 5, May 2001 Page(s):797 - 802

AbstractPlus | References | Full Text: PDF(192 KB) IEEE JNL

16. **Bidirectional systolic arrays for digital recursive filters**
Sousa, L.A.;
Electronics, Circuits and Systems, 1998 IEEE International Conference on
Volume 3, 7-10 Sept. 1998 Page(s):499 - 502 vol.3
AbstractPlus | Full Text: PDF(372 KB) IEEE CNF

17. **Digit-serial modular multiplication using skew-tolerant domino CMOS**
Kim, S.; Sobelman, G.E.;
Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP '01). 2001 IEI
Conference on
Volume 2, 7-11 May 2001 Page(s):1173 - 1176 vol.2
AbstractPlus | Full Text: PDF(280 KB) IEEE CNF

18. **An adaptable binary entropy coder**
Kiely, A.; Klimesh, M.;
Data Compression Conference, 2001. Proceedings. DCC 2001.
27-29 March 2001 Page(s):391 - 400
AbstractPlus | Full Text: PDF(500 KB) IEEE CNF

19. **An analysis of perceptual artifacts in MPEG scalable audio coding**
Creusere, C.D.;
Data Compression Conference, 2002. Proceedings. DCC 2002
2-4 April 2002 Page(s):152 - 161
AbstractPlus | Full Text: PDF(717 KB) IEEE CNF

20. **A power-aware IP core design for the variable-length DCT/IDCT targeting at MPE adaptive transforms**
Kuan-Hung Chen; Jiun-In Guo; Jinn-Shyan Wang; Ching-Wei Yeh; Tien-Fu Chen;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Sympos
Volume 2, 23-26 May 2004 Page(s):II - 141-4 Vol.2
AbstractPlus | Full Text: PDF(266 KB) IEEE CNF

21. **Implementation of a low complexity, low power, integer-based turbo decoder**
Wu, P.H.-Y.; Pisuk, S.M.;
Global Telecommunications Conference, 2001. GLOBECOM '01. IEEE
Volume 2, 25-29 Nov. 2001 Page(s):946 - 951 vol.2
AbstractPlus | Full Text: PDF(1120 KB) IEEE CNF

22. **A versatile and scalable digit-serial/parallel multiplier architecture for finite fields**
Hutter, M.; Grossschadl, J.; Kamendje, G.-A.;
Information Technology: Coding and Computing [Computers and Communications], 20
ITCC 2003. International Conference on
28-30 April 2003 Page(s):692 - 700
AbstractPlus | Full Text: PDF(344 KB) IEEE CNF

23. **Systematic design of pipelined recursive filters**
Lapointe, M.; Huynh, H.T.; Fortier, P.;
Computers, IEEE Transactions on
Volume 42, Issue 4, April 1993 Page(s):413 - 426
AbstractPlus | Full Text: PDF(1056 KB) IEEE JNL

24. **A floating-point processor for fast and accurate sine/cosine evaluation**
Paliouras, V.; Karagianni, K.; Stouraitis, T.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [s
and Systems II: Express Briefs, IEEE Transactions on]

Volume 47, Issue 5, May 2000 Page(s):441 - 451
AbstractPlus | References | Full Text: PDF(368 KB) IEEE JNL

25. **Fast algorithm for modular reduction**
Kop, Q.K.; Hung, C.Y.;
Computers and Digital Techniques, IEE Proceedings-
Volume 145, Issue 4, July 1998 Page(s):265 - 271
AbstractPlus | Full Text: PDF(636 KB) IEE JNL

View: 1·

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 18775 | "708"/$.ccls. and @ad<"20020122" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:50 |
| L2 | 728 | 1 and interleav$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:50 |
| L3 | 587 | 2 and (alu$1 or (arithmetic near$2 logic)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:51 |
| L4 | 314 | 3 and "and" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:51 |
| L5 | 37 | 4 and slic$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:53 |
| L6 | 1 | 5 and 708/490.ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:52 |
| L7 | 0 | 5 and 708/700-714.ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:52 |
| L8 | 0 | 5 and 708/200.ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:52 |

| | | | | | | |
|---|---|---|---|---|---|---|
| L9 | 27 | arrang$3 and 5 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/06 10:54 |